ABSTRACT

During fabrication of a mask read-only memory (ROM) device, a dielectric layer is grown on a substrate. Strip-stacked layers are formed on the dielectric layer, with each strip-stacked layer including a polysilicon and a silicon nitride layer. Source/drain regions are formed in the substrate between the strip-stacked layers, and spacers are then deposited between the strip-stacked layers. The strip-stacked layers are patterned into gates, which are disposed over every code position, with silicon nitride pillars being disposed on the gates. Additional spacers are formed on gate sidewalls. The silicon nitride pillars are removed, exposing the gates. A mask is then formed to cover active code positions, in accordance with the desired programming code. Insulating layers are then deposited through the mask onto the exposed gates. When the mask is removed, word lines are formed, interconnecting the gates without the insulating layers.